CMOS Image Sensors: Electronic Camera on A Chip

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Abstract

Recent advancements in CMOS image sensor technology arc reviewed, including both passive pixel sensors and active pixel sensors. On-chip analog to digital converters and on-chip timing and control circuits permit realization of an electronic camera-on-a-chip.

1. Introduction

Today there are many kinds of electronic cameras with very different characteristics. Camcorders arc the most well known electronic camera and capture images with television resolution at 30 frames per second. The camcorder market has driven impressive improvements in charge-coupled device (CCD) technology - the ubiquitous electronic camera sensor technology. Digital still cameras capture higher resolution images (e.g. 1024 x 1024 or higher) at slower pixel rates. These cameras, while presently very expensive for consumer applications, are expected to rapidly drop in price. Low resolution monochrome CCD cameras are very inexpensive. Spaceborne, high resolution electronic cameras occupy the opposite cod of the spectrum.

Ncw markets arc emerging for digital electronic cameras, especially in computer peripherals for document capture and visual communications. If the cost of tbc camera can be made so fficiently low (e.g. $100 or less per camera) it is expected that most personal computers will have at least one camera peripheral. Even less expensive cameras will find automotive and entertainment applications. Wireless applications of cameras will require ultra low power operation. Very small cameras (e.g. less than JO cm^3) will also permit new markets.

Despite the wide variety of applications, all digital electronic cameras have the same basic functions. These arc(I) optical collection of photons, i.e. a lens, (2) wavelength discrimination of photons, i.e. filters, (3) detector for conversion of photons 10 electrons e.g. a photodiode, (4) a method to readout the detectors e.g. a CCD, (5) timing, control and drive electronics for the sensor, (6) signal processing electronics for correlated double sampling, color processing, etc., (7) analog to digital conversion and (8) interface electronics, In a CCD-based system, these electronics often consume several Walls of power (e.g. 5 W-1 O W) and, for example, are the major drain on a camcorder battery. The volume anti mass of the electronics and power supply constrains the level of miniaturization achievable with the system.

Since the CCD's inception in the early 1 970's, the main focus of research and development has been CCD sensor performance. Criteria include quantum efficiency, optical fill factor (fraction of pixel used for detection), dark current, charge transfer efficiency, readout noise, readout rate, lag, smear, and dynamic range. A desire to reduce optics mass has driven a steady reduction in pixel size. HDTV and scientific applications have driven an inci case in array size. Recently, emphasis has been placed on functionality, soch as electronic shutter, low pow cr and simplified supply voltages.

CMOS image sensors, under sporadic investigation since the 1960's, and under-nourished in comparison to CCDs, are very apropos for highly integrated, low power imaging systems. I Historically, CMOS image sensors have compared on favorably to CCDs with respect to the above performance criteria. However, recent advances have led to the CMOS active pixel sensor (AI'S) that has performance competitive with CCDs but with vastly inci cased functionality, substantially lower system power (1 0-50 mW), and the potential for lower system cost.

It is now straightforward to envision a single chip camera that has integrated timing and control electronics, sensor array, signal processing electronics, analog to digital converter and interface. Such a camera-on-a-chip will have a full digital interface, operate with standard logic supply voltages, and consume power measured in the tens of milliwatts. This paper describes CMOS image sensor technology and the roadmap to achieve a cal~lcra-orl-a-chip imaging system.

2.1 Historical Background

Before CMOS APS and before CCDs there was MOS. in the 1960's there were numerous groups working on solicl-state image sensors with varying degrees of success using NMOS, PMOS and bipolar processes. For example, in 1963, Morrison reported a structure (that is now referred to as a computational sensor) that allowed determination of a light spot's position using the photoconductivity effect [1]. The *scanistor* was reported in 1964 by IBM [2]. The scanistor used an array of npn junctions addressed through a resistive network to produce an output pulse proportions] to the local incident light intensity. In 1966 Westinghouse reported a 50x50 clement monolithic array of phototransistors [3]. All of these sensors had an output signal proportional 10 the instantaneous local incident light intensity and did not perform any intentional integration of the optical signal. As a consequence, the sensitivity of these devices was low and they required gain within the pixel to enhance their performance.

in 1967, Weckler at Fairchild suggested operating p-n junctions in a photon flux integrating mode [4]. The photocurrent from the junction is integrated on a reverse-biased p-n junction capacitance. Readout of the integrated charge using a PMOS switch was suggested. The signal charge, appearing as a current pulse, could be converted to a voltage pulse using a series resistor. A 100x 100 element array of photodiodes was reported in 1968 [5]. Weckler later called the device a *reticon* and formed Reticon to commercialize the sensor.

Also in 1967, RCA reported a thin-film transistor ('1'1"1') solid-state image sensor using CdS/CdSe TFTs and photoconductors [6]. The 180x180 element array included self-scanning complementary logic circuitry for sequentially addressing pixels. A battery operated wireless camera was also reported to have been constructed to demonstrate the array.

Also active at that time was Plessey in the UK. In a 1968 seminal paper, Noble dcscribcd several configurations of self-scanned silicon image detector arrays [7]. Both surface photodiodcs and buried photodiodcs (to reduce dark current) were described. Noble also discussed a charge integration amplifier for readout, similar to that used later by others. in addition, the first usc of a MOS source-follower transistor in the pixel for readout buffering was reported. An improved model and description of the operation of the sensor was reported by Chamberlain in 19698. The issue of fixed-pattern noise (FPN) was explored in a 1970 paper by Fry, Noble, and Rycroft [9].

Until recently, FPN has been considered the primary problem with MOS and CMOS image sensors. in 1970, when the CC I) was first reported [10], its relative freedom from FPN was onc of the major reasons for its adoption over the many other forms of solid-state image sensors. The smaller pixel size afforded by the simplicity of the CCI) pixel also contributed to its embrace by industry.

The 1970's saw a great deal of activity in CCDs but little reported activity on other image sensors. In the late 197o's and early 1980's I litachi continued the development of MOS image sensors [11] for camcorder-type applications, including single chip color imagers [12]. Temporal noise in h40S sensors started to lag behind the noise achieved in CCDs, and by 1985, Hitachi combined the MOS sensor with a CCD horizontal shift register [13]. in 1987, I litachi introduced a simple on-chip technique to achieve variable exposure times and flicker suppression from indoor lighting [14]. 1 lowever, perhaps duc to residual temporal noise, especially important in low light conditions, Hitachi abandoned its MOS approach to sensors.

3. Modern CMOS image sensors

The 1990's have seen a resurgent interest in CMOS image sensors. The major reason for the interest is related to miniaturized and cost effective imaging systems. CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on-chip and reduce component and packaging costs. CCD technology, on the other hand, has become quite specialized and, in general, is not well-suited to CMOS integration duc to voltage, capacitance and process constraints.

Contributing to the recent activity in CMOS image sensors is the steady, exponential improvement in CMOS technology. The rate of minimum feature size decrease has outpaced similar improvements in CCD technology. Furthermore, sensor pixel size is limited by both optical physics and optics cost, making moot the CCD's inherent pixel size advantage. Recent progress in on-chip signal processing, has also reduced F1'N to acceptable levels.

There arc three predominant approaches to pixel implementation in CMOS: passive pixel, photodiode-type active pixel, and photogate-ty pe active pixel. These arc described below. '1'here are also several ways to make pn junction photodiodes in CMOS [15], but generally n-l diodes on a p/p+ epi substrate in an n-well process give the most satisfactory results.

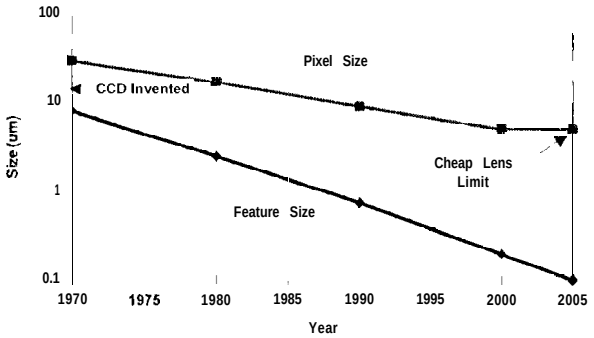

Figure 1. The steadily increasing ratio between pixel size and minimum feature size permits the use of CMOS circuitry within each pixel.

Passive pixel approach

The passive photodiode pixel approach remains virtually unchanged since first suggested by Weckler in 1967. The passive pixel concept is shown below in Figure 2 and is the basis for photodiode arrays produced by EG&G Reticon and Hitachi, and more recently, by Edinburgh University and VLSI Vision in Scotland[16,17], and by Linkoping University and IVP in Sweden[18,19,20]. Significant levels of integration have been achieved with the passive pixel approach, including on-chip analog-to-digital conversion (ADC) described later.

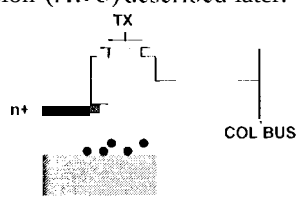

Figure 2. Passive pixel schematic and potential well. When the transfer gate TX is pulsed, photogenerated charge integrated on the photodiode is shared on the bus capacitance.

The passive pixel features excellent quantum efficiency since the photodiode is not covered by polysilicon. With only a single transistor per pixel required for readout, it has the smallest possible pixel pitch for a given optical fill factor. A second selection transistor has sometimes been added to permit true X-Y addressing and reduce bus capacitance. Pixel pitch is typically 10x the minimum feature size. Small pixels are desired for small inexpensive die size and small, lightweight optics.

Much larger pixels have been used for document imaging[21]. Page-sized image sensors (7.7" x 9.6") using amorphous silicon and constructed with a passive pixel architecture have been demonstrated with a dynamic range of 104-10[5].

The major problems with the passive pixel are its noise level and scalability. Noise on a passive pixel is typically of the order of 250 electrons r.m.s., compared to commercial CCDs that achieve less than 20 electrons r.m.s. of read noise. The passive pixel also does not scale well to larger array sizes and or faster pixel readout rates. This is because increased bus capacitance and faster readout speed both result in higher readout noise. To date, passive pixel sensors suffer from large fixed pattern noise, though this is not a fundamental problem.

Active pixel approach

It was quickly recognized, almost as soon as the passive pixel was invented, that the insertion of a buffer/amplifier into the pixel could potentially improve the performance of the pixel. A sensor with an active amplifier within each pixel is referred to as an active pixel sensor or APS. Since each amplifier is only activated during readout, power dissipation is minimal and generally less than a CCD. Non-CMOS AI'S devices have been developed that have excellent performance such as the charge-modulation devices (CMD)[22] but these devices[23,24,25] require a specialized fabrication process. In general, AI'S technology has many advantages over CCDs.[26]

The CMOS AI'S trades pixel fill factor for improved performance using the in-pixel amplifier. Pixels are typically designed for a fill factor of 20-30%. Loss in optical signal is more than compensated by reduction in read noise for a net increase in signal to noise ratio and dynamic range. Microlenses are commonly employed with low fill factor interline CCDs[27,28] and can recover the lost optical signal. The simple, polyimide microlense refracts incident radiation from the circuitry region of the pixel to the detector region. The microlense can improve optical fill factor by 3-fold so that the net optical aperture for the detector is 60%-80%.

Photodiode-type AI'S

The photodiode-type AI'S was described by P. Noble in 1968 and has been under investigation by F. Andoh at NHK in Japan since the late 1980's[29,30,31] in collaboration with Olympus, and later, Mitsubishi Electric. A diagram of the photodiode-type APS is shown below in Figure 4. In a version of the NHK/Olympus device, the photodiode is not used for optoelectronic conversion; instead an a-Se thin film covers the pixel and the sensor is operated in an electron-bombarded mode. A similar device with an a-Si:H overlayer was described by Huang and Ando in 1990[32] but operated in a conventional optically illuminated mode. The overlayer is used to improve

effective fill factor. The structure of Figure 4 was also employed by JPL in a 128x128 element array that bad on-chip timing, control, correlated double sampling and fixed pattern noise suppression circuitry[33], as shows in Figure 5.

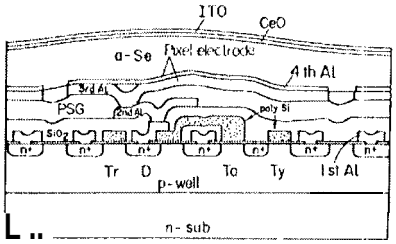

Figure .?, ('rosssection o f NIIK CMOS A PS structure with a-Se overlayer for electron bombardme nt from photocathode.

More complicated pixels can be constructed to improve functionality and to a lesser extent, performance. I lamamatsu reported on an improved sensor that used a transfer gate between the photod iodc and the source follower gate[34]. The transfer gate keeps the photodiode at constant potential and increases output conversion gain by reducing capacitance but introduces lag. The 1 lamamatsu sensor also improved fixed pattern noise using a feedback technique. More complication was added by the Technion to permit random access and electronic shuttering at a significant expense of pixel size[35].

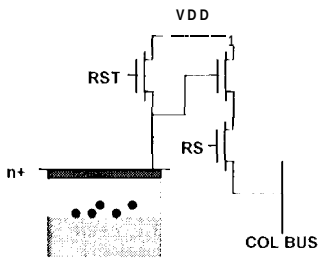

Figure 4. A photodiode-type active pixel sensor (APS). The voltage on the photodiode is buffered by a source follower to the column bus, selected by RS-row select. The photodiode is reset by transistor RST.

l'hoto(iiodc-type AI'S pixels have high quantum efficiency as there is no overlying polysilicon. The read noise is limited by tbc reset noise on the photodiode since correlated double sampling is not easily implementable, and is typically 75-100 electrons r.m s. The photodiodc-type APS uscs three transistors pcr pixel and has a typical pixel pitch of 15x tbc minimum feature size. The photodiode AI'S is suitable for most mid to low performance applications, and its performance improves for smaller pixel sizes since the reset noise scales as $C^{1/2}$, where C is the photodiodc capacitance. Preliminary measurements at J] 'l, indicate that the dark current radiation sensitivity of the photodiodc-type AI'S is superior to tbc pbotogatc-type APS described next.

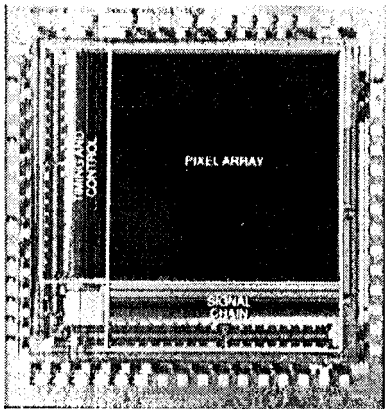

Figure 5. A 128x128 photodiode-type CMOS AI'S with on chip timing control, correlated double sampling and fixed pattern mist suppression ciruitry. Readout window and interframe integration time is asynchronously commanded. JPL chip requires only + 5V and clock /0 produce high quality analog video output[33].

Photogate-type APS

The photogate AI'S was introduced by J] 'l, in1993[36,37] for high performance scientific imaging and low light applications. The photogate APS combines CCD benefits and X-Y readout, and is shown schematically below in Figure 6. Signal charge is integrated under a photogate. For readout, an output floating diffusion is reset and its resultant voltage measured by the source follower. The charge is then transferred to the output diffusion by pulsing the photogate. The new voltage is then sensed. The difference between the reset level and the signal level is the output of the sensor. This correlated double sampling suppresses reset noise, 1/f noise, and fixed pattern noise duc to threshold voltage variations.

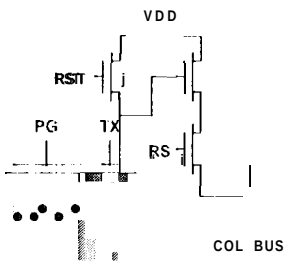

Figure 6. Photogate-type APS pixel schematic and potential wells. Transfer of charge and correlated double sampling permits low noise operation.

The photogate and transfer gate ideally overlap using a double poly process. However, the insertion of a floating diffusion between PG and TX has minimal effect on circuit pet-rormancc and permits the usc of single poly processes[38]. The photogatc-type APS uscs five transistors per pixel and has a pitch typically equal to 20x the minimum feature size. Thus, to achieve a 10 µm pixel pitch, a 0.5 µm process must be employed.

A 0.25 μm process would permit a 5 μm pixel pitch. The floating cliff ision capacitance is typically of the order of 10 fF yielding a conversion gain of 10-20 μV/electron. Subsequent circuit noise is of the order of 150-250 μVr.m.s., mulling in a readout noise of 10-20 electrons r.m s., with the lowest noise demonstrated to date of 13 electrons r.m s.[39]

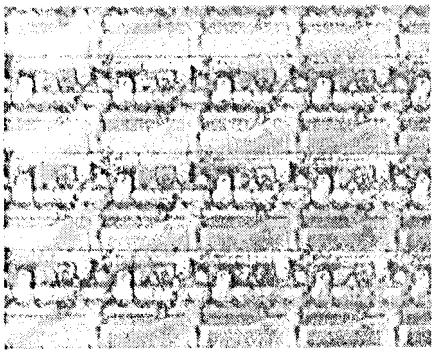

Figure 7. Close up of photogate pixels implemented using 1.2 μm design rules with 20.4 μm pixel pitch by JPL.

The architecture of the CMOS APS is typically designed to read out a row at a time, as selected by a decoder, with the reset and signal levels held on sampling capacitors at the bottom of the column. The column capacitors arc selected by a decoder for buffered readout. '1'bus, the sensor can be read out in a sequential or nearly random access subsampled fashion, or by selecting a small window for readout to enable electronic zoom.

Figure 8. Image of a US $1 bill taken with a JPL 256x256 element CMOS APS showing excellent image quality with no artifacts.

A 256x256 CMOS AI'S with 20 μm pixels implemented using 0.9 μm CMOS, without timing and control was reported by AT&T and JPL[40]. Motion detection was implemented by changing the timing of the sensor so that the previous frame is stored on the floating diffusion while the next frame is integrated under the photogate. Output is the difference between successive frames. A 1024x IO24 element CMOS AI'S with 10 μm pixels implemented using 0.5 μm CMOS, also without timing and control, bas beta fabricated and tested and will be reported soon by AT&T and JPL[41]. A 256x256 element CMOS AI'S with 20.4 μm pixels implemented using a 1.2 μm n-well process with timing and control logic will be reported by JPL[39]. This sensor requires only +5V and clock to produce analog video output. Variable integration time and window of interest readout can be commanded asynchronously. The chip can be readout in normal mode or in motion detection mode.

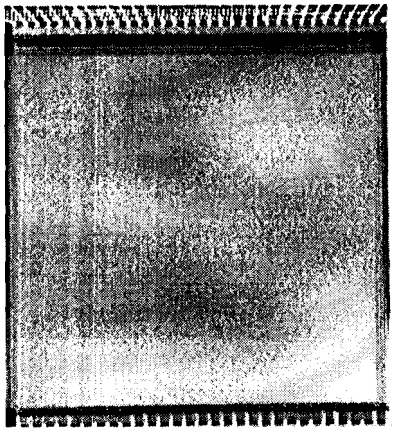

Figure 9. 1024x1024 element photogate CMOS APS with 10 μm pixel pitch fabricated using 0.5 μm design rules by AT&T/JPL.

Other pixel.y

A non-integrating 512x512 clement photodiodc-type APS was reported by IMEC with a 6.6 μm pixel pitch[42]. This sensor operates in a non-integrating current mode with logarithmic response. FPN was corrected by means of bot-carrier-induced threshold voltage shift.

The pinned photodiode, developed for interline transfer CCDs, features high quantum efficiency (esp. in the blue), low dark current, and low noise readout. The pinned photodiode has been combined with CMOS APS readout by JPL/Kodak to achieve high performance pixel response[43]

A photogate CMOS AI'S with a floating-gate sense amplifier that allows multiple non-destructive, doubly sampled reads of the same signal was developed by JPL for usc with oversampled column-parallel ADCs[44].

A floating gate sensor with a simple structure was reported by JPL/Olympus[45]. This sensor used a floating gate to collect and sense the photosignal and features a compact pixel layout with completer reset.

'1'here has been significant work on retina-like CMOS sensors with]lon-linear, adaptive response[46]. While their utility for electronic image capture has not yet been demonstrated, their very large dynamic range and similarity to the response of the human eyc offer intriguing possibilities for on-chip intelligent imaging.

Analog signal processing

On-chip analog signal processing can be used to improve the performance and functionality of the CMOS image sensor. JPL has developed a delta-difference sampling (DDS) approach to suppress FPN peak-to-peak to 0.1 % of saturation level[33]. Other examples of signal processing demonstrated in CMOS image sensors include smoothing using neuronMOSFETs[47], programmable amplification[48], multiresolut ion imaging[49], video compression[50], and intensity sorting[51]. Continued improvement in analog signal processing performance and functionality is expected. Other computatimal-type opt ical sensors have been demonstrated that use CMOS analog signal processing[52,53].

On-chip ADC

On-chip ADC is desired for image sensors to simplify system design and achieve a single chip imaging system. One of the most significant benefits of a CMOS-based image sensor is its easy integration with an on-chip analog-to-digital converter. The ADC must have low power dissipation, not occupy too much chip area, yet achieve at least 8 bit resolution at 10 megapixel/sec data rates. Many different architectures are possible as the design trade space is relatively flat[54]. It is possible to have a single ADC for the entire array operating at high conversion rate, an ADC for each pixel operating at the frame rate, or an AD C for each column of the array. The latter architecture is referred to as column-parallel and represents a good trade of parallelism and chip area for lower power. Several Swedish papers have been presented that described column-parallel ADCs integrated with passive pixel CMOS image sensors[18,19,20]. These sensors generally use the single-slope ADC conversion technique. A column parallel 8-bit single slope Al) C has been integrated with a small CMOS APS by JPL[55], and a larger array with the same ADC was demonstrated by JPL/AT&T[56]. Since the CMOS AI'S has a dynamic range of 13-14 bits, greater resolution is desirable. Oversampled ADCs in a column parallel architecture were demonstrated by Mendis at JPL[44,55] but not integrated with an image sensor. Pixel level oversampled ADC has been explored by Stanford[57] but requires high frame rate readout, A single-bit ADC integrated with a pbotodiodc-type CMOS APS was developed for high speed binary imaging[58].

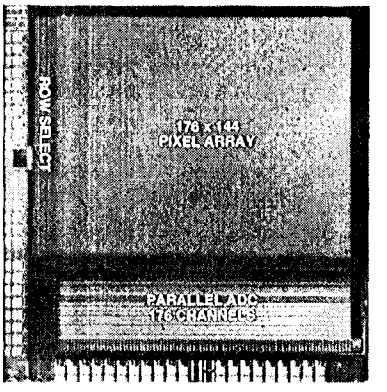

Figure 10. A 176x144 element, 20 µm pitch CMOS APS with 176 8-b single slope ADCs achieving 30 Hz operation with 35 mW power at 3.5 1 supply voltage by A T & T.

4. Roadmap for Camera-on-a-Chip

All the component technologies to realize a CMOS electronic can]cra-on-a-chip have been developed. Single chip cameras based on the lower performance passive pixel are already available. Higher performance single-chip cameras based on the CMOS APS technology are expected t o emerge shortly. Improvement in on-chip ADC technology to take advantage of the high dynamic range is needed. Backend processes for color filter arrays and microlenses are nearly as complicated as the standard CMOS process and add significantly to cost. A single chip color camera can be expected in the next year or two. Standards for digital cameras need to be developed to enable the wider development of the technology.

4. Impact of CMOS Scaling Trends

The future prospects for CMOS image sensors are bright. The effect of predictable trends in CMOS technology, based on the industry standard technology roadmap, wer c examined by Fossum and Wong of JPL/IBM[59]. To at least 0.25 µm minimum feature sizes, it appears that the standard CMOS process will permit the fabrication of high performance CMOS image sensors.

The most obvious problem, but the easiest to correct, is the trend toward the use of silicides. Silicides are optically opaque and detrimental to image sensing. A silicide-blocking mask is available in some processes already. The switchover to silicon-on-insulator (S01) technology will be problematic for the sensors due to the minimal absorption of photons in thin silicon films, bat such a switchover is not expected to generally occur until

beyond 0.25 μm minimum feature sizes. Active pixel sizes al the "cheap lens limit" (e.g. 5 pm) will bc readily achievable in 0.25 μm CMOS. Passive pixel sizes well below that size will also bc achievable.

Below 0.25 μm, "off" transistor currents may bc of concert], Dark current is expected to minimally increase from 0.5 μm processes to 0.25 μm processes. This will likely bc compensated by a steady improvement in wafer and process quality control. intrinsic fixed pattern noise may increase due to threshold voltage mismatch, but FPN suppression circuitry will likely become more sophisticated as well. A switch from LOCOS to shallow trench isolation would likely improve sensor performance. Deep trench isolation would be useful to reduce crosstalk. Reduced power supply voltages will reduce analog circuitry "headroom", but is partially offset by concomitant reduction in threshold voltages. Increases in DRAM chip size will drive improvements in process control as well as stepper field size -- useful for larger format image sensors.

It is inevitable that when CMOS image sensors capture a significant share of the electronic imaging market, process deviations from standard CMOS will be made to permit product different i at ion and improved performance. This is already the case with analog CMOS for capacitors and isolation. Use of the pinned photodiode[43] will improve quantum efficiency and decrease dark current. Double poly will permit efficient implementation of capacitors. I lowever, the increased integration and low power enabled by CMOS will continue to permit many advantages over a CC1)-based technology.

5. Conclusions

Highly miniaturized imaging systems based on CMOS image sensor technology are emerging as a competitor to CCDs for low cost visual communications and multimedia applications. The CMOS active pixel sensor (AI'S) technology has demonstrated noise, quantum efficiency, and dynamic range performance comparable to CCDs with greatly increased functionality. CMOS image sensors with on-chip timing and control, and analog-to-digital conversion are enabling one-chip imaging systems with a fall digital interface. Such a "camera-on-a-chip" may make image capture devices as ubiquitous in oar daily lives as the microprocessor.

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Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, dots not constitute or imply its endorsement by the United States Government, or the Jet Propulsion 1.abor'story, California Institute of Technology.

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